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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,200	10/21/2003	Salman Akram	4244.5US (97-1355.05/US)	3680

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,200	AKRAM ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 6-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claim 6 requires a sequence in which a conformal layer is deposited (corresponding to figure 3 without the doping region 16a); a single layer sidewall spacer is deposited, and a first doping step is performed (corresponding to figure 5, where doping region 17a is provided); the single layer sidewall spacer is formed into another spacer having a smaller thickness, and then a second doping step is performed (corresponding to figure 6, where doping regions 17a and 18a are provided); and substantially removing the another single layer sidewall spacer and performing a third doping (corresponding to figure 4, where the third doping region is 16a). The specification, however, does not teach or suggest this claimed sequence, but rather only suggests a sequence corresponding to figures 3, 4, 5, 6 in order, or a sequence of figures 3, 4, 6, 5, in order. In fact, the specification provides no suggestion that the innermost (i.e., closest to the gate structure, aligned with the 'substantially removed another single layer sidewall spacer') implant step (corresponding with implant 16a) could be performed after the outer implants. Hence, the

specification does not reasonably convey that the Applicant, at the time of invention, had possession of the specific claimed method sequence.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the steps of substantially removing the third sidewall spacer; and introducing a third dopant into the substrate to form the third subregion, the third subregion *being generally aligned with the second sidewall.* It is not clear from the claim language or the disclosure exactly what is encompassed by "generally aligned," and whether such a limitation means that the third subregion is actually aligned with the first single thin layer sidewall spacer, which is fairly thin, and thus taken as being "generally aligned with the second sidewall", whether the subregion is actually aligned with the second sidewall, thus requiring a removal of the first single thin layer sidewall spacer (which is neither claimed nor disclosed) before implanting the third subregion, or whether an angled implant or other similar technique (also neither claimed nor disclosed) is used to form a subregion aligned with the second sidewall that is covered by the first single thin layer sidewall spacer. For the purposes of examination, it is assumed that subregions aligned with the first single thin layer sidewall spacer are taken as being "generally aligned with the second sidewall."

Claim 6 further recites the limitation of "a gate oxide formed on the dielectric layer." It is not clear as to what is meant by this limitation, since the drawings, specification, and general state of the art would suggest that the gate oxide layer is formed directly on the substrate and is a part of the dielectric layer, rather than being formed on the dielectric layer. It is further unclear as to what is meant by a gate structure including a gate oxide layer and a metal silicide layer formed on the gate oxide layer, since the gate structure would need to be conductive in order to function and would typically be formed from polysilicon or metals. It is assumed for the purposes of examination that the gate oxide is part of the dielectric layer, and the gate structure includes a polysilicon or metal layer capped with a metal silicide, in order to correspond with the structure disclosed in the specification of the present application (see, for example, paragraph 0028).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,866,460 to Akram et al. (cited by applicant) in view of U.S. Patent No. 6,187,645 to Lin et al. (cited by applicant).

Regarding claims 6 and 10, Akram discloses a method for making a transistor comprising: providing a substrate (10); forming a dielectric layer (14) on a portion of the

substrate (column 4, lines 9-11); forming a gate structure on the dielectric layer (see column 4, lines 23-55) having a transition layer (20) formed on the dielectric layer and a metal silicide layer (22) formed on the transition layer (figure 2a), the gate structure having first and second sidewalls (21), the sidewalls defining therebetween first and second contact regions (40) and a channel region (15); forming first (40), second (34), and third (16) subregions within the second contact region (figure 2c), each subregion having a dopant concentration that differs from that of the other two subregions (column 6, lines 20-35), where the process of forming the subregions comprises: forming a single layer sidewall spacer (26; figure 2a) made of silicon nitride or silicon oxide (column 5, lines 60-67) having a large thickness overlying the first and second sidewalls; introducing a first dopant into the substrate to form the first region (40; column 7, lines 20-27); forming the single layer sidewall spacer into another single layer sidewall spacer (26 in figure 2b; see column 7, lines 27-30), the 'another single layer sidewall spacer' having a thickness smaller than the thickness of the single layer sidewall spacer (figures 2a-2b); introducing a second dopant (34; figure 2b); substantially removing the 'another single layer sidewall spacer' (see figure 2d); and introducing a third dopant (16 in figure 2d) into the substrate to form the third subregion, the third subregion being substantially aligned to the sidewalls of the gate structure.

Akram fails to disclose depositing a conformal layer of dielectric material having a first thickness on the sidewalls and thus 'under' the single layer sidewall spacer, and then subjecting the conformal layer to an annealing/oxidation process.

Lin discloses forming a very thin conformal layer (308) on the sidewalls of a gate structure and underneath the source/drain implant spacer layer (316), such that the LDD implant

(314) is spaced apart from the sidewalls of the gate structure by the width of the conformal spacer (see figure 3c). Lin further discloses anisotropically etching the conformal layer (column 4, lines 37-41) and subjecting the conformal layer to an annealing/oxidation process (column 4, lines 42-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Akram, such that a very thin conformal layer is deposited, anisotropically etched, and annealed before depositing the sidewall spacer layers, as suggested by Lin. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a conformal layer between the gate sidewalls and the implant spacer layer of Akram, because in Akram, the implant region extends entirely to the sidewall of the gate structure (see Akram, figure 2d). Lin, however, teaches that such a configuration is not desirable, since having the implant region aligned with the sidewalls of the gate structure leads to diffusion of dopants underneath the gate structure, and hence a gate-to-drain capacitance in the device (see Lin, column 1, lines 30-45; column 2, lines 14-23). Since the inclusion of a thin conformal spacer layer on the sidewalls, such that the innermost implant is aligned to the conformal layer rather than to the sidewalls, leads to a reduction in the diffusion of ions into the channel region under the gate structure, and hence to a reduction in the gate-to-drain capacitance (see Lin, column 2, lines 14-25; 55-67), it is well within the purview of a person skilled in the art to add such a feature to the method of Akram, in order to achieve this advantage. Furthermore, it would have been obvious to include the anisotropic etching and annealing/oxidation steps taught in Lin, since a person having ordinary skill would naturally turn to the teachings of Lin for forming the conformal layer of Lin, and to achieve the additional benefit of clearing away crystal

defects on the substrate surface and within the gate structure, thus improving the performance of the device (see Lin, column 4, lines 42-53).

Regarding claims 7-9, Akram fails to specifically disclose the thicknesses of the sidewalls.

Lin suggests that spacer dimensions are selected to minimize drain capacitance (see column 1, lines 35-45; column 2, lines 14-24) and to set the length of the LDD region (see figures 1A-C; 3A-E). Lin further teaches that the first spacer thickness is about 150 angstroms (column 3, lines 45-50), and that the second spacers are wider tan the first spacers (figures 3A-3E).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the first spacer of Akram as modified by Lin is about 150 angstroms, and that the second spacer is significantly wider, as suggested by Lin. The rationale is as follows: A person having ordinary skill in the art would have been motivated to a first spacer of about 150 angstroms, and a second spacer of 550 angstroms, because doing so enables one to confine the dopant spread in the LDD to areas not under the gate region, and thus prevent undue gate-to-drain capacitance (Lin, column 1, lines 35-45; column 2, lines 14-24). Additionally, selecting a relatively large second spacer thickness allows one to control the distance between the heavily doped drain region and the channel region, thus preventing dopants from the heavily doped regions from migrating to the gate/channel regions (see figures 1 and 3 of Lin). Although neither Akram nor Lin specifically teach the thickness of the second spacer, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to

discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

Response to Arguments

7. Applicant's arguments filed 11/25/05 have been fully considered but they are not persuasive.

The cancellation of claims 1 and 5 in response to the 35 U.S.C 112 rejections is noted. The Examiner further notes, however, that the Applicant has simply re-introduced the claim language previously rejected under 35 U.S.C. 112 first paragraph into new claim 6 without arguing as to why the rejection was not proper. Hence, the exact same 112 first paragraph rejection applied against claims 1 and 5 in the 8/22/05 Office Action is considered to apply to claims 6-10.

The Applicant further argues that the rejection based on Akram and Lin does not teach all of the claim limitations. This argument is not persuasive, because the Applicant fails to specifically point out the claimed elements not present in Akram and Lin. The Applicants further make the allegation that any combination of the cited prior art merely teaches or suggests the prior art of Figure 1 of the Applicant's disclosure modified using hindsight from Lin to arrive at the claimed invention. This argument is not persuasive, because Akram teaches the concepts of disposing a sidewall spacer on a gate structure, performing an implant, reducing the thickness of the spacer; performing another implant; substantially removing the spacer, and then performing another implant (see the figures 2A-2D sequence, for example). The only thing missing in Akram is the concept of adding a thin, conformal sidewall spacer under the sidewall

spacer of Akram, such that the implants are separated from the sidewall of the gate structure. Since Lin clearly teaches adding a thin, conformal sidewall spacer to separate the implanted region from the sidewall of the gate structure in order to achieve the benefits of reducing the gate-to-drain capacitance and leakage under the gate region, the Examiner maintains that a combination of Akram and Lin is proper. The Examiner is mystified as to the Applicant's assertion that "any combination of the cited prior art merely teaches or suggests the prior art illustrated in drawing Fig. 1 of the Applicants' disclosure modified using hindsight from the teachings of the Lin et al. reference, since figure 1 only shows a gate structure having a single implant aligned to a single sidewall spacer, which is not particularly close or relevant to the claimed material, and not remotely as relevant as the cited Akram and Lin references.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

Carl Whitehead

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